What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a main surface and a back surface, including a first region, a second region and a third region, and having a first semiconductor layer of a first conductivity type formed over the main surface;

a second semiconductor layer of a second conductivity type opposite to the first conductivity type formed over the first semiconductor layer in the first region;

a plurality of first groove portions penetrating, in the first region, through the second semiconductor layer from the main surface of the semiconductor substrate;

a first insulating film formed in the first groove portions;

a first conductor formed over the first insulating film;

a third semiconductor layer formed, in the second semiconductor layer, adjacent to the first groove portions and having the first conductivity type;

a second groove portion formed in the second region;

a second insulating film formed in the second groove portion;

a second conductor formed over the second insulating film and electrically connected to the first conductor; and

a plurality of fourth semiconductor layers of second

conductivity type formed over the first semiconductor layer in the third region,

wherein the second groove portion is adjacent to the second semiconductor layer and the fourth semiconductor layer, and

wherein the second semiconductor layer and the fourth semiconductor layer each has a first impurity concentration and a first depth.

2. A semiconductor device according to Claim 1, including an MISFET having the first semiconductor layer as a drain, the second semiconductor layer as a channel, the third semiconductor layer as a source and the first conductor layer as a gate.

3. A semiconductor device according to Claim 2,

wherein the first semiconductor layer, the third semiconductor layer and first conductor are electrically connected to drain electrode, source electrode and gate electrode, respectively, and

wherein the second semiconductor layer and the third semiconductor layer are electrically connected via the source electrode.

4. A semiconductor device according to Claim 3, wherein the plurality of fourth semiconductor layers are field limiting rings encompassing the first region and second region when viewed from the top.

5. A semiconductor device according to Claim 3, wherein the plurality of fourth semiconductor layers prevent lowering in the breakdown voltage between the source electrode and drain electrode.

6. A semiconductor device according to Claim 3, wherein when a reverse bias is applied to the drain and channel, depletion layers extending from the second semiconductor layer and fourth semiconductor layer are connected with each other.

7. A semiconductor device according to Claim 3, wherein the fourth semiconductor layer is electrically connected with the third conductor in the third region.

8. A semiconductor device according to Claim 3, wherein when reverse bias is applied to the drain and channel, the breakdown voltage in the second region is equal to or higher than a breakdown voltage lower of the breakdown voltage in the first region and the breakdown voltage in the third region.

9. A semiconductor device according to Claim 3, wherein the breakdown voltage between the source electrode and drain electrode is 100V or greater.

10. A semiconductor device according to Claim 3,

wherein the second conductor in the second region extends in a first direction which is parallel to the main surface of the semiconductor substrate,

wherein the second conductor has a first portion extending in a direction vertical to the main surface of the semiconductor substrate and a second portion extending in a second direction which is parallel to the main surface of the semiconductor substrate and at the same time crosses the first direction, and

wherein the width of the second portion parallel to the second direction is not greater than $3.80 + 0.148\rho$ (μm) in which the resistivity of the first semiconductor layer is represented by ρ ($\Omega \cdot$ cm).

11. A semiconductor device according to Claim 3,

wherein the second conductor in the second region extends in a first direction which is parallel to the main surface of the semiconductor substrate,

wherein the second conductor has a first portion extending in a direction vertical to the main surface of the semiconductor substrate and a second portion extending in a second direction which is parallel to the main surface of the semiconductor substrate and crosses the first direction;

wherein a third insulating film is formed between the second portion and the main surface of the semiconductor substrate, and

wherein the width of the third insulating film parallel to the second direction is not greater than 3.80

+ 0.148ρ (μm) wherein the resistivity of the first semiconductor layer is represented by ρ(Ω · cm).

12. A semiconductor device according to Claim 3, wherein a plurality of the first conductors extend in a second direction which is parallel to the main surface of the semiconductor substrate.

13. A semiconductor device according to Claim 12, wherein the first conductor also exists in a first direction which is parallel to the main surface of the semiconductor substrate and crosses the second direction.

14. A semiconductor device according to Claim 3,

wherein the first conductor has a third portion extending in a direction which is parallel to the main surface of the semiconductor substrate and extends in a direction crossing an extending direction of the second conductor, and a fourth portion extending in a direction which is parallel to the main surface of the semiconductor substrate and in an extending direction of the second conductor, and

wherein the fourth portion is disposed between the second conductor and the third semiconductor layer.

15. A semiconductor device comprising:

a semiconductor substrate having a main surface and a back surface, including a first region, a second region and a third region, and having a first semiconductor layer of a

first conductivity type formed over the main surface;

a second semiconductor layer formed over the first semiconductor layer in the first region and having a second conductivity type opposite to the first conductivity type;

a plurality of first groove portions penetrating, in the first region, through the second semiconductor layer from the main surface of the semiconductor substrate;

a first insulating film formed in the first groove portions;

a first conductor formed over the first insulating film;

a third semiconductor layer formed, in the second semiconductor layer, adjacent to the first groove portion and having the first conductivity type;

a second groove portion formed in the second region;

a second insulating film formed in the second groove portion;

a second conductor formed over the second insulating film and electrically connected to the first conductor;

a plurality of fourth semiconductor layers of second conductivity type formed over the first semiconductor layer in the third region; and

in the first region, a trench gate type MISFET having the first semiconductor layer as a drain, the second semiconductor layer as a channel, the third semiconductor

layer as a source and the first conductor as a gate,

the semiconductor device further comprising:

a gate extraction portion comprised of the second conductor and field limiting rings comprised of the plurality of fourth semiconductor layers and encompass the first region and the second are when viewed from the top,

wherein the second semiconductor layer and the plurality of the fourth semiconductor layers are formed in one step.

16. A manufacturing method of a semiconductor device having a trench gate type MISFET, a gate extraction portion for the trench gate type MISFET and a field limiting ring in a first region, a second region and a third region of a semiconductor substrate, respectively, comprising the steps of:

(a) forming a first semiconductor layer of a first conductivity type over the main surface of the semiconductor substrate;

(b) forming a first groove portion and a second groove portion in the first region and the second region, respectively, over the main surface of the semiconductor substrate;

(c) forming an insulating film in the first groove portion and the second groove portion;

(d) forming a conductor over the insulating film;

(e) after the step (d), implanting an impurity of a second conductivity type opposite to the first conductivity type into the semiconductor substrate in the first region to form a second semiconductor layer of the second conductivity type over the first semiconductor layer in the first region, and implanting an impurity of the second conductivity type opposite to the first conductivity type into the semiconductor substrate in the third region to form a fourth semiconductor layer of the second conductivity type over the first semiconductor layer in the third region; and

(f) implanting an impurity of the first conductivity type into the second semiconductor layer to form therein a third semiconductor layer of the first conductivity type adjacent to the first groove portion,

wherein the second semiconductor layer is formed so that the first groove portion penetrates through the second semiconductor layer,

wherein in the first region, the trench gate type MISFET having the first semiconductor layer as a drain, the second semiconductor layer as a channel, the third conductor layer as a source and the conductor in the first region as a gate, and

wherein the field limiting ring is formed to encompass the first region and the second region from the

fourth semiconductor layer, when viewed from the top.

17. A manufacturing method of a semiconductor device according to Claim 16, wherein the conductor in the second region has a first width in the second groove portion and a second width outside the second groove portion and the conductor is formed so that the second width exceeds the first width.

18. A manufacturing method of a semiconductor device according to Claim 16, wherein the second semiconductor layer and the fourth semiconductor layer are formed in one step.

19. A manufacturing method of a semiconductor device having a trench gate type MISFET, gate extraction portion for the trench gate type MISFET and field limiting ring in first, second, and third regions of the semiconductor substrate, respectively, comprising the steps of:

(a) forming a first semiconductor layer of a first conductivity type over the main surface of the semiconductor substrate;

(b) implanting an impurity having a second conductivity type opposite to the first conductivity type into the semiconductor substrate in the first region to form a second semiconductor layer of the second conductivity type over the first semiconductor layer in the first region, and implanting an impurity of the second

conductivity type opposite to the first conductivity type in the semiconductor substrate in the third region to form a fourth semiconductor layer of the second conductivity type over the first semiconductor layer in the third region;

(c) after the step (b), forming a first groove portion and a second groove portion in the first region and the second region, respectively, over the surface of the semiconductor substrate;

(d) forming an insulating film in the first groove portion and the second groove portion;

(e) forming a conductor over the insulating film; and

(f) implanting an impurity of the first conductivity type into the second semiconductor layer and thereby forming therein a third semiconductor layer of the first conductivity type which is adjacent to the first groove portion,

wherein the first groove portion is formed to penetrate through the second semiconductor layer,

wherein in the first region, the trench gate type MISFET having the first semiconductor layer as a drain, the second semiconductor layer as a channel, the third semiconductor layer as a source, and the conductor in the first region as a gate is formed, and

wherein the field limiting ring encompassing the first

region and the second region is formed from the fourth semiconductor layer when viewed from the top.

20. A manufacturing method of a semiconductor device according to Claim 19, wherein the second semiconductor layer and the fourth semiconductor layer are formed in one step.